Scaling Challenges and Device Design Requirements for High Performance Sub-50 nm Gate Length Planar CMOS Transistors

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Abstract

We investigate scaling challenges and outline device design requirements needed to support high performance-low power planar CMOS transistor structures with physical gate lengths (L_{GATE}) below 50nm. This work uses a combination of simulation results, experimental data and critical analysis of published data. A realistic assessment of gate oxide thickness scaling and maximum tolerable oxide leakage is provided. We conclude that the commonly accepted upper limit of 1A/cm^2 for gate leakage is overly pessimistic and that leakage values of up to 100A/cm^2 are deemed acceptable for future logic technology generations. Unique channel mobility and junction edge leakage degradation mechanisms, which become prominent at 50nm L_{GATE} dimensions, are highlighted using quantitative analysis. Source-drain extension (SDE) profile design requirements to simultaneously minimize short channel effects (SCE) and achieve low parasitic resistance for sub-50nm L_{GATE} transistors are described for the first time.

Scaling Issues & Device Requirements

Table 1 summarizes key transistor scaling requirements for 70-180nm logic technology nodes. The projections are based on extrapolating results from 180nm logic technology node published by this group and other industry leaders [1-3]. Given limited room for further V_{TH} scalability due to static power considerations, the supply voltage is expected to scale by only 0.8x per generation to maintain an acceptable gate overdrive (Fig. 1). Electrical oxide thickness is projected to scale by 0.8x per generation to maintain reliability [constant $V_{DD}/T_{OX}(e)$]. SDE depth and under-diffusion are projected to scale by 0.7x per generation to control SCE and support L_{GATE}. Channel doping projections are commensurate with gate oxide scaling requirements. A comprehensive analysis of scaling issues and device design requirements is presented next.

(a) Gate Oxide Scaling: Fig. 2 shows gate oxide leakage (J_{OX}) dependence on physical T_{OX-EFF} for pure SiO_2 and nitrided-SiO_2 gates. Pure SiO_2 leakage data is extracted from Ref. [4] and incorporates V_{DD} scaling with T_{OX} from Table 1. More than 10x J_{OX} reduction relative to pure oxide is observed at the same physical T_{OX-EFF} for optimized nitrided-SiO_2 [3]. This data point is used together with the J_{OX} vs. T_{OX-EFF} slope already obtained for pure oxide to project gate leakage values for future nodes for devices with nitrided-SiO_2 gate. Fig. 3 shows computed transistor sub-threshold (I_{OFF}) and I_{GATE} components of static leakage at 25^o C and 100^{o}C vs. L_{GATE} for an inverter with FO=3. Leakage calculations assume nitrided-SiO_2 and use the I_{OFF} and T_{OX} parameters listed in Table 1. Experimentally measured temperature acceleration factors are used to determine I_{OFF} at 100^{o}C. Fig. 4 shows that I_{GATE} is 7x lower than I_{OFF} at 100^{o}C (product operating temperature) at the 50nm L_{GATE} node, and has a J_{OX} of ~100A/cm^2. Circuit simulations using I_{OFF} values from Table 1 and 100A/cm^2 gate leakage, show acceptable functionality and noise margin for both static and domino circuits at the 50nm L_{GATE}. This analysis enables us to conclude that the nitrided-SiO_2 gate can be extended to the 50nm L_{GATE} node and that J_{OX} leakage of ~100 A/cm^2 is feasible for logic products as long as it meets reliability criteria. Furthermore, as evident from I_{GATE}/I_{OFF} ratio of >1 at 100^{o}C, a high-k dielectric will be necessary for the 35nm L_{GATE} node.

(b) Mobility Degradation: Fig. 5 shows a plot of E_{EFF} in a Si inversion layer (at V_{DD}) vs. channel doping for 35nm-100nm L_{GATE} transistors. Maximum NMOS channel doping, prior to the onset of channel impurity scattering dominated mobility, is extracted for various E_{EFF} (Si) from published data [5] (Fig. 5). Unlike previous generations, this plot illustrates that the electron mobility will become dominated by channel impurity scattering even up to $V_G=V_{DD}$ for the 35nm L_{GATE} node. Fig. 6 shows the impact of remote charge scattering from ionized dopants in poly-Si on mobility at $V_G=V_{DD}$. This data has been extracted from Ref. [6] and highlights the need for a high-k dielectric at a 35nm L_{GATE}.

(c) Junction Edge Leakage: Fig. 7 shows measured NMOS gated-edge junction leakage (I_{JE}) vs. channel doping (N_{CH}) for $N_{CH} \geq 10^{18}$ cm^{-3}. I_{JE} is dominated by the tunneling component and is expected to limit the maximum channel doping to ~5x10^{18} cm^{-3} to maintain $I_{JE}<I_{OFF}$. This most likely will negate potential solutions for mitigating mobility losses due to impurity dominated scattering, such as a vertical retrograde channel profile, as discussed above.

(d) SDE Profile Requirements: The importance of lateral SDE profile abruptness is quantified by simulating devices with gaussian SDE doping profiles in both the vertical and lateral directions. Simulation results in Fig. 8 indicate that for current 100nm L_{GATE} devices, the minimum PMOS SDE gate under-diffusion prior to the onset of rapid I_{DSAT} degradation is 15-20 nm/side. This limit is specific to devices formed by the "implant+anneal" SDE process and concurs with the results published in Ref. [7]. Furthermore, we show for the first time, the minimum SDE under-diffusion limit can be significantly improved to below 10nm/side by increasing SDE lateral abruptness (expressed as the approximate distance in nm per decade drop in doping concentration) 2x relative to current devices (Fig. 8). Fig. 9 shows that the lower limit for SDE depth without significantly increasing R_{SDE} is ~40nm for current 100nm L_{GATE} devices and highlights the importance of achieving super-active SDE concentration by a non-equilibrium formation process. Fig. 10 shows SDE lateral abruptness requirements needed to maintain the R_{SDE} of the 100nm L_{GATE} device down to 35-100nm L_{GATE} nodes. SDE depth and under-diffusion requirements are incorporated from Table 1. Various SDE active doping values are also considered to explore the trade-off between doping and lateral abruptness. These results indicate that in order to maintain a constant R_{SDE} from the 100nm L_{GATE} node down to the 35nm L_{GATE} (which has a 20nm SDE depth and 8 nm/side under-diffusion), 3x improvement in SDE lateral abruptness is required. To obtain 0.7x R_{SDE} improvement per generation, hyper-abrupt SDE junctions with better than 0.2 nm/dec lateral abruptness is needed at the 35nm L_{GATE} node (Fig. 11).

Conclusions

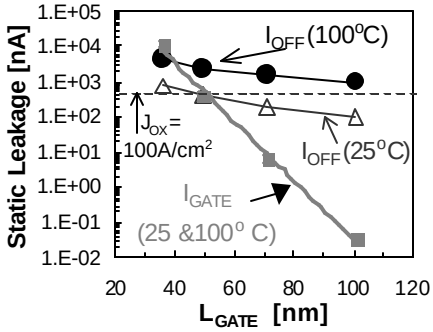
In this work, a nitrided-SiO_2 gate dielectric was shown to be feasible down to a 50nm L_{GATE} and up to 100A/cm^2 gate leakage is allowable from relative static power and circuit functionality considerations. At a L_{GATE} of 35nm, channel impurity scattering was projected to dominate mobility, but gated junction leakage limits using retrograde profiles as a potential solution. Finally, SDE profile requirements for continued parasitic resistance scaling down to a 35nm L_{GATE} were provided for the first time.

References

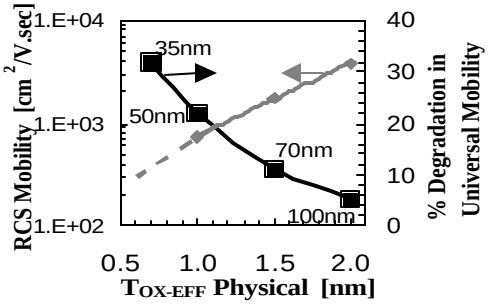
[1] T. Ghani et al., *IEDM Tech. Digest*, pp. 415, 1999.
[2] M. Hargrove et. al, *IEDM Tech. Dig.*, pp. 627, 1998.
[3] M. Rodder et al., *IEDM Tech. Digest*, pp. 623, 1998.
[4] S. H. Lo et al., *IEEE Electron Device Letters*, pp. 209, 1997.
[5] S. Takagi et al., *IEDM Tech. Digest*, pp. 398, 1988.
[6] M. Krishnan et al., *IEDM Tech. Digest*, pp. 571, 1998.
[7] S. Thompson et al., *Symp. VLSI Tech. Dig.*, pp. 132, 1998.

Generation [nm]	180	130	100	70	Scaling Factor
L_{GATE} [nm]	100	70	50	35	0.7x
V_{DD} [Volts]	1.5	1.2	1.0	0.8	0.8x
Tox(e) [nm] Tox (Phys) [nm]	3.1 2.1	2.5 1.5	2.0 1.0	1.6 0.6	0.8x
SDE depth [nm]	50	35	24	17	0.7x:
SDE Under-Diff [nm]	23	16	11	8	0.7x:
L_{MET} [nm]	55	40	27	20	0.7x:
Channel Doping [$x10^{18}$ cm^{-3}]	1	1.6	2.6	4	$1/(0.8)^2$ =1.6x
I_{DSAT} [Relative]	1	1	1	1	1x
I_{OFF} [nA/μm] [25° C]	20	40	80	160	2x

Table 1. Scaling projection of transistor paramete for future logic technology generations.



°C and 100°C for an inverter driving identical gate load with FO=3. Inverter W_N=1μm and W_P=2μm.



universal mobility for pure SiO_2 due to RCS at V_G=V_{DD} for 35-100nm L_{GATE} (extracted from [6]).

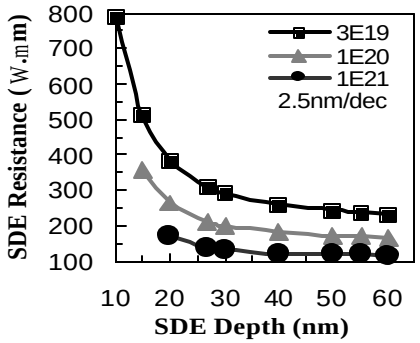


Fig. 9. PMOS SDE resistance(R_{SDE}) vs. SDE junction depth for three different SDE doping levels.

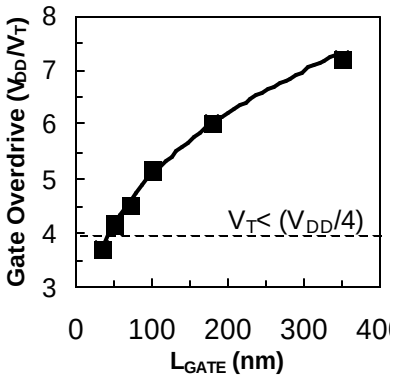
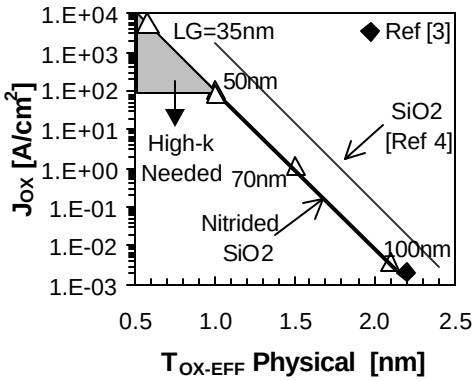


Fig.1 successive generations. Gate overdrive limitation to slow V_{DD} scaling.



physically effective oxide thickness (EOT) for pure and nitrided oxides.

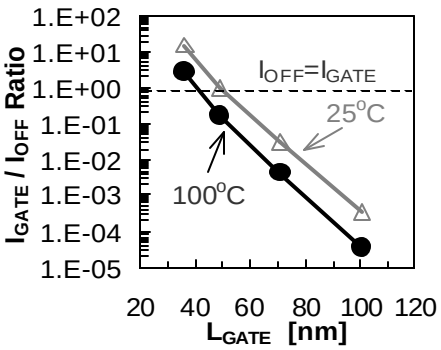


Fig. 4. I_{GATE}/I_{OFF} Ratio at 25° C and 100° C for the circuit described in caption of

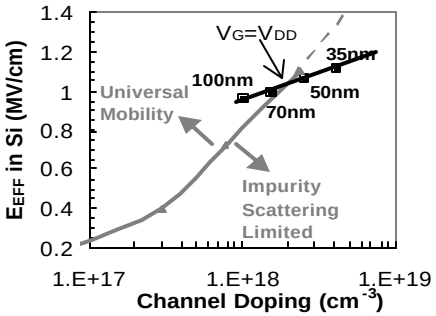
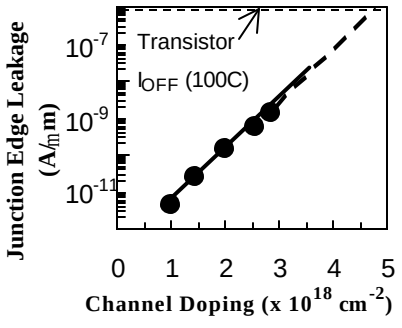


Fig. 5 Universal mobility vs. channel impurity scattering dominated regimes. Device falls off the universal mobility controlled regime for 35nm L_{GATE}.



leakage vs. channel doping for NMOS devices. Transistor I_{OFF} at 100°C for 35nm L_{GATE} also shown for reference.

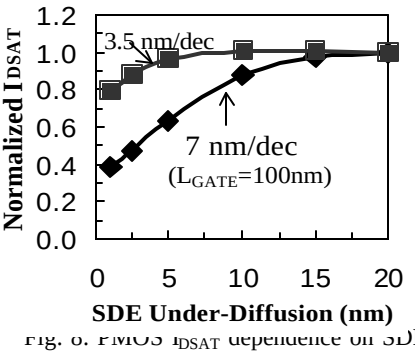


Fig. 8. PMOS I_{DSAT} dependence on SDE under-diffusion for two different SDE lateral profile abruptness values.

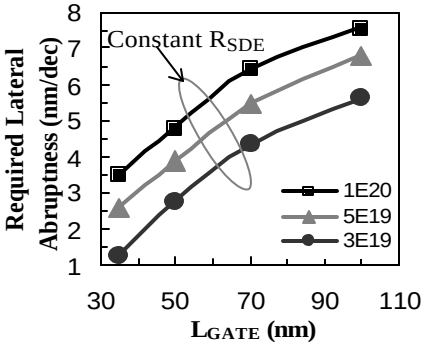
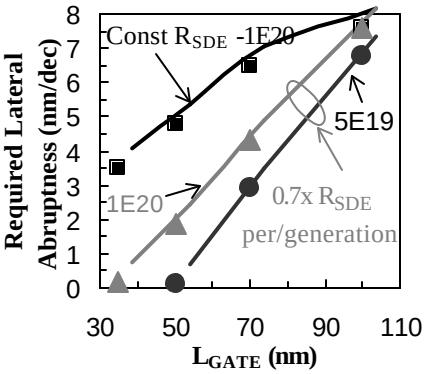


Fig 10. PMOS SDE lateral abruptness requirement for 35-100nm L_{GATE} for constant R_{SDE} scaling scenario and with active doping as a parameter.



requirement for 35-100nm L_{GATE} for constant vs. 0.7x R_{SDE} scaling per generation.